CLAIMS

What is claimed is:

1. An integrated memory device that comprises:
   a nonvolatile memory array; and
   a nonvolatile buffered memory interface integrated on a substrate with said memory array, wherein the memory interface comprises:
      one or more volatile buffers configured to buffer data for read operations; and
      a table memory configured to indicate one or more addresses associated with data buffered in the one or more volatile buffers.

2. The device of claim 1, wherein the table memory is volatile, and wherein the memory interface is configured to preserve contents of the table memory in nonvolatile memory during absences of electrical power.

3. The device of claim 2, wherein the memory interface is further configured to restore the contents of table memory from the nonvolatile memory when electrical power returns.

4. The device of claim 1, wherein when electrical power returns, the memory interface is further configured to restore the one or more volatile buffers to a state preceding the absence of electrical power.

5. The device of claim 1, wherein the one or more volatile buffers comprise:
   a plurality of read buffers each associated with a different region of the memory array and configured to buffer only data for read operations on an associated region.

6. The device of claim 1, wherein the memory array comprises magnetic random access memory (MRAM) cells.

7. The device of claim 1, wherein the memory interface further comprises:

an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to the memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands.

8. The device of claim 7, further comprising:

an error correction code (ECC) decoder coupled between the memory array and the one or more volatile buffers.

9. A method of providing access to stored data, the method comprising:

preserving during an absence of electrical power information indicative of data in one or more read buffers; and

restoring the data to the one or more read buffers when power returns.

10. The method of claim 9, wherein said preserving comprises:

detecting a pending power-down;

for each of the one or more read buffers, storing in nonvolatile memory a starting address associated with data in the read buffer.

11. The method of claim 10, wherein said restoring comprises for each of the one or more read buffers:

accessing the nonvolatile memory to retrieve the starting address associated with the read buffer; and

filling the read buffer with data from a memory array, beginning with data associated with the starting address.

12. The method of claim 10, wherein before said detecting the method further comprises:

receiving a read command that comprises a read address;

determining whether data from the read address is buffered in a read buffer;

retrieving data from a location in a memory array associated with the read address if the data is not buffered; and

responding to the read command with data from said one of the plurality of read buffers if the data is buffered.

13. A method of providing access to stored data, the method comprising:

preserving during an absence of electrical power information indicative of data in one or more read buffers;

when power returns, determining whether a restore operation is enabled; and

if the restore operation is enabled, restoring the data to the one or more read buffers when power returns.

14. The method of claim 13, wherein the one or more read buffers are integrated on a substrate with a nonvolatile memory array, and wherein said restoring comprises for each of the one or more read buffers:

retrieving a start address from nonvolatile memory; and

filling the read buffer with data retrieved from the nonvolatile memory array starting at the start address.

15. A digital device that comprises:

a memory having a nonvolatile buffered memory interface with one or more read buffers; and

a processor coupled to the memory device and configured to retrieve stored information from the memory,

wherein the processor causes the memory to receive a power down command before electrical power is removed from the memory, and wherein the memory interface responsively stores in a nonvolatile memory information indicative of data in said one or more read buffers.

16. The device of claim 15, wherein the memory interface is further configured to reload the one or more read buffers with data in accordance with information from the nonvolatile memory when power returns.

17. The device of claim 15, wherein the information stored in the nonvolatile memory comprises a starting address for each of the one or more read buffers.

18. The device of claim 15, wherein the one or more read buffers comprise:

a plurality of read buffers each associated with a different region of the memory and configured to buffer only data for read operations on an associated region.

19. The device of claim 18, wherein the memory interface further comprises:

an interface control module that is configured to receive read commands specifying a memory address, wherein the interface control module is coupled to a nonvolatile memory array to conduct read operations to satisfy the read commands and to prepare read buffers to satisfy anticipated read commands; and

wherein the memory further comprises:

an error correction code (ECC) decoder coupled between the nonvolatile memory array and the one or more read buffers.